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08EC009

M.Tech. Degree Examination, December 2010
Advances in VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***1.Answer any FIVE full questions.***
2. Missing data, if any, may be suitably assumed.

1 a. Draw the transfer plot of CMOS inverter. Discuss the effect of aspect ratio on the transfer curve, with suitable mathematical analysis. **(08 Marks)**

b. Derive an expression for drain current in MESFET, below pinch off. **(08 Marks)**

c. Bring out the differences between BiCMOS and CMOS technology. **(04 Marks)**

2 a. A n-channel Si JFET has $N_A = 10^{19}$ cm^{-3}, $N_D = 5\times10^{15}$ cm^{-3}, L = 30 μm, z = 200 μm, a = 1.5 μm. Assume $M_n = 1350$ cm^2/vs. Determine
i) Built in voltage ii) The pinch off voltage iii) Drain current at $V_{GS} = 0V$, $V_{DS} = 4V$
iv) $V_{D(sat)}$ for $V_{GS} = 0V$, $V_{GS} = -2V$ v) $I_{D(sat)}$ for $V_{GS} = -2V$ **(10 Marks)**

b. Describe the construction and working principle of MESFET. **(10 Marks)**

3 a. Derive an expression for the threshold voltage of a MIS structure. Also, comment on the sign of V_T. **(10 Marks)**

b. A n-channel MOSFET has $N_a = 5\times10^{19}$ cm^{-3}, $M_n' = 500$ cm^2/Vs , $Q_{ms} = -0.96V$, $Q_i = 5\times10^{10}$ q/cm^2, z = 100 μm, d = 30 nm, L = 5 μm, $n_i = 10^{10}$ cm^{-3}, $K_o = 3.9$, $K_S = 11.9$.
i) Determine the drain current at gate voltage $V_G = 2V$ and a drain voltage $V_D = 1V$.
ii) Consider the case, where, the gate voltage is 3V and the drain voltage in 4V. **(10 Marks)**

4 a. Discuss the small signal operation of MESFET. Derive the expression for cutoff and maximum operating frequency of MESFET. **(08 Marks)**

b. Calculate the cutoff frequency of a MOSFET, given that L = 2 μm, $M_n' = 1350$ cm^2/Vs, $V_G = 5V$ and $V_T = 1.5V$. **(04 Marks)**

c. Describe the short channel effects as applied to MOS circuit. **(08 Marks)**

5 a. Show that the threshold voltage and drain current scale linearly with dimensions and voltage in constant electric field scaling method. Also, mention the problems of constant electric field scaling, in brief. **(10 Marks)**

b. Explain the working of a carbon nanotube FET device, with a neat sketch. **(06 Marks)**

c. List the key advantages of materials, used for molecular computing. **(04 Marks)**

6 a. Construct a 2 i/p AND gate and OR gate, using diodes. **(05 Marks)**

b. Explain the working of inverting NMOS super buffer. Draw the circuit and stick diagram. **(05 Marks)**

c. Explain the design of pass transistor logic. Design a NMOS pass transistor logic for an XNOR gate. Write the truth table and K-map. **(10 Marks)**

7 a. Realize the following:
i) $Z = \overline{A(P+E)+BC}$, using the static CMOS AOI technology. Draw the circuit diagram and stick diagram.
ii) Draw the circuit diagram for $Y = \overline{a+b(c+d)}$, using the static NMOS technology. **(10 Marks)**

b. Realize the XOR and XNOR gates, using CMOS transmission gates. **(06 Marks)**

c. Explain global routing and local routing. **(04 Marks)**

8 a. With an example, explain the terms hierarchy, regularity, modularity and locality. **(10 Marks)**

b. Write explanatory notes on :
i) Programmable logic structure ii) Gate array standard cell design. **(10 Marks)**

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